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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/872,209

06/01/2001

R. Daniel McGrath

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1987

3897

7590

02/13/2003

SCHNECK & SCHNECK
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EXAMINER

YAM, STEPHEN K

ART UNIT

PAPER NUMBER

2878

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,209

Applicant(s)

MCGRATH ET AL.

Examiner

Stephen Yam

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This action is in response to Amendments and remarks filed on December 10, 2002. Claims 1-9 are currently pending.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should include attributes suggesting a "user interface" or "user control" of the invention.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara European Patent Application No. EP-0942592 in view of Noble et al. US Patent No. 5,760,636.

Shinohara teach (see Fig. 4) an integrated imager system having an array of pixel areas (30) with at least one control area (4), wherein said pixel areas include a plurality of light collecting elements (see Col. 3, lines 1-6) which each receive and store electronic information in an amount indicative of an amount of light received during an integration period, with the control area having an internal timing element (7), with an interface (3, 6, 10, 13, 20) for receiving a

Art Unit: 2878

plurality of data, address, and control signals, said interface receiving a mode signal (10) (see Col. 3, lines 19-23) for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses (see Col. 4, lines 3-9) the internal timing element (7) to control timing operation of the system and the second operating mode bypasses (see Col. 4, lines 20-22) the internal timing element to control timing operation of the system. Regarding Claim 2, Shinohara teach (see Fig. 4) the control area including a data bus (20), an address and control bus (3) (see Col. 3, lines 54-58) electrically coupled to the interface and a bypass multiplexer (9) connected to the control bus, said multiplexer operating to interconnect the internal timing element (7) to the control bus upon receipt of a first mode signal and operating to bypass the internal control element upon receipt of a second mode signal (see Col. 3, lines 19-23). Regarding Claim 3, Shinohara teach (see Fig. 4 and Col. 4, lines 20-22) means for receiving timing signals from an external timing element (2) when the system is operating in the second operating mode. Regarding Claim 4, Shinohara teach (see Fig. 4 and Col. 4, lines 29-33) the external timing block (2) including a color recovery block. Since Shinohara teach (see Col. 3, lines 8-10) the external timing element (2) outputting drive pulses for the second operating mode, it is inherent that the external timing element (2) includes an external timing generator. Regarding Claim 5, Shinohara teach (see Fig. 4) the external timing block (2) comprising a microcomputer. It is inherent that a microcomputer includes a memory for data storage and a DMA interface block for controlling external devices. Regarding Claim 6, Shinohara teach (see Col. 3, lines 24-29) the imager operating in the first operating mode when the interface is not connected to receive the mode signal. Shinohara does not teach the interface as a user interface configured to receive the mode signal from a user. Noble et al. teach (see Fig. 1) a

Art Unit: 2878

microprocessor (10) with a user interface (12) wherein the clock frequency ("Clock Frequency") is adjusted based on a mode signal (SLOW#) received from a user (see Col. 3, lines 46-49 and Col. 6, lines 21-29) to provide user control of power consumption (see Col. 6, lines 24-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a user interface receiving a mode signal from a user as taught by Noble et al. in the system of Shinohara, to provide customized user control of power consumption to best suit a user's particular needs, as taught by Noble et al. (see Col. 6, lines 26-29).

3. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara. Shinohara teach (see Fig. 3) a timing selector for an integrated imager, comprising an onboard timing means (7) associated with a integrated imager (1), for providing standard timing signals to operate a clock circuit (7, 8, 21) aboard the integrated imager (1) and an outboard logic circuit (2) electrically connected to the integrated imager generating signals for establishing timing signals for customized imager operation. Shinohara also teach the outboard logic circuit (2) performing (see Col. 4, lines 29-33) image signal processing such as color processing, white balancing, etc., and turning off the microcomputer to save power (see Col. 4, lines 34-40). Regarding Claim 8, Shinohara teach (see Fig. 3) the outboard logic unit (2) outputting drive pulses- therefore, it is inherent that the outboard logic unit (2) includes means for generating clock signals for bypassing the clock circuit (see Col. 3, lines 44-51). Regarding Claim 9, Shinohara teach (see Fig. 3 and Col. 3, lines 24-29) the outboard logic circuit having means (10) for generating clock signals using the clock circuit (7, 8, 21). Shinohara do not teach a user establishing timing signals and a user interface allowing selection of the onboard timing means

Art Unit: 2878

or outboard logic circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to establish a user interface to allow selection of the onboard timing means or outboard logic circuit and allow a user to establish timing signals in the timing selector of Shinohara, to allow user control of power consumption from the microprocessor and activation/deactivation of the image processing functions provided by the microprocessor to provide a more user-flexible system.

Response to Arguments

4. Applicant's arguments filed December 10, 2002 have been fully considered but they are not persuasive.
5. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Regarding Claims 7-9, Applicant argues that hindsight is used to assume a user input for power consumption for the device of Shinohara is obvious. Examiner asserts that user control of the power consumption characteristics of electronic devices has been well known and in public use, ranging from the user-controlled dimming of laptop screens and digital camera displays to reduce LCD power usage, to Intel's SpeedStep™ technology, described in Noble et al. US Patent No. 5,760,636, describing a user control for the clock speed of a laptop CPU. Hence, Examiner maintains that providing a user input for controlling power consumption for the device of Shinohara is not hindsight and hence, remains obvious under 35 U.S.C. 103(a).

Conclusion

Art Unit: 2878

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Art Unit: 2878

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703)308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

SY
January 29, 2003



DAVID PORTA
SUPERVISORY PATENT EXAMINER
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